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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,581	07/16/2003	Hwa Sung Rhee	SEC.891D	7431

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,581	RHEE ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 13-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 22-30 is/are allowed.

6)☒ Claim(s) 13-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/16/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the divisional filed 7/16/2003.

Currently, claims 13-30 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 13 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al. (U.S. Patent No. 6,373,112 filed 12/2/1999) in view of Wu (U. S. Patent No. 5,773,348 patented 6/30/1998).

Murthy shows the method substantially as claimed and as described in Figs. 1-5 and corresponding text as: depositing a gate insulating layer (104) over a surface of a semiconductor substrate (102) (col. 4, lines 7-19); depositing a lower poly-SiGe layer (112) having a columnar crystalline structure over the gate insulating layer... (col. 4, lines 7-19) (claims 13). Murthy shows that prior to crystallizing the amorphous Si Layer, patterning the lower poly-SiGe layer and the amorphous Si later to define a gate electrode (col. 4, lines 6-32) (claim 18). Murthy shows that after crystallizing the amorphous Si layer, patterning the lower poly-SiGe layer and the upper poly-Si layer to define a gate electrode (col. 4, lines 6-32) (claim 19). Murthy shows that a seed layer is deposited on the surface of the semiconductor layer prior to depositing the lower poly-SiGe layer (col. 3 line 52- col. 4 line 4) (claim 20).

Murthy lacks anticipation only in not explicitly teaching that: 1) an amorphous Si layer is deposited over the lower poly-SiGe layer and the amorphous Si layer is crystallized to obtain an upper poly-Si layer having a random crystalline structure (claim 13); 2) the amorphous Si layer is crystallized by an anneal process (claim 21).

Murthy shows that a poly-SiGe layer is used as a lower gate electrode and is set under an upper poly-Si gate electrode (col. 5, lines 10-21).

Wu teaches in a similar device, a method of using an amorphous silicon gate that is annealed to form a polysilicon gate (col. 5, lines 8-14). Wu uses these fabrication methods in order to prevent the substrate from being damaged (col. 2, lines 1-4). The amorphous layer then can be annealed in either a separate thermal process or salicide (col. 5, line 8-14).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Murthy, by using the amorphous Si layer to form a poly-Si as described in Wu by replacing the polysilicon deposition process used by Murthy, with the motivation that the annealing of the amorphous silicon will cause less damage to the substrate.

4. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al. (U.S. Patent No. 6,373,112 filed 12/2/1999) in view of Wu (U. S. Patent No. 5,773,348 patented 6/30/1998) as applied to claim 13 above, and further in view of Schinella (U.S. Patent No. 6,730,588 filed 12/20/2001).

Murthy and Wu show the method substantially as claimed and as described in the preceding paragraphs.

Murthy and Wu lack anticipation only in not explicitly teaching that: 1) the lower poly-SiGe layer is deposited by CVD at a temperature range of 400°C to 600°C(claim 14); 2) the lower poly-SiGe layer is deposited by chemical vapor deposition of SiH_4 and GeH_4 at a temperature range of 400°C to 600°C (claim 15); and the lower poly-SiGe layer is deposited by chemical vapor deposition of Si_2H_6 and GeH_4 at a temperature range of 400°C to 600°C (claim 16).

Schinella teaches in a similar gate electrode formation, the use of Si containing gases and GeH_4 in CVD methods used to deposit a poly-SiGe layer (col. 4, lines 39-51). It is suggested that the silicon germanium deposition be carried out at temperatures of 300°C to 800°C (col. 4 line 32- col. 5 line 3). The silicon gate electrodes are formed using a thin nucleation layer (col. 1, lines 7-10).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method shown in the combination of Murthy and Wu, by depositing the poly-SiGe layer in a manner taught by Schinella, with the motivation that the selective deposition of the gate electrode can be etched by short, controllable etch sequences. Additionally, the gas mixture is only deposited on the gate electrode nucleation layer but fails to deposit on the gate dielectric layer, which increases the stability of the dielectric layer.

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al. (U.S. Patent No. 6,373,112 filed 12/2/1999) in view of Wu (U. S. Patent No. 5,773,348 patented 6/30/1998) as applied to claim 13 above, and further in view of Yu (U.S. Patent No. 6,743,680 filed 6/22/2000).

Murthy and Wu show the method substantially as claimed and as described in the preceding paragraphs.

Murthy and Wu lack anticipation only in not explicitly teaching that: the amorphous Si layer is deposited by CVD at a temperature range of 350 °C to 580°C.

Yu teaches in a similar gate electrode formation, an amorphous silicon layer that is deposited at a temperature of 400-450°C (col. 5, lines 48-52). The amorphous silicon layer is deposited in the above range. It is well known in the art that amorphous silicon is deposited in the range of 350°C to 580°C.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method shown in the combination of Murthy and Wu, by depositing the amorphous silicon layer in a manner taught by Yu, with the motivation

that the selective deposition of the gate electrode can be etched by short, controllable etch sequences. Additionally, the temperature range of deposition of the amorphous layer is below the crystallization temperature of silicon (580°C).

Allowable Subject Matter

6. Claims 22-30 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...depositing at least one intermediate layer having an amorphous structure over the lower poly-SiGe layer;

depositing an amorphous Si layer over the at least one intermediate layer; and

crystallizing the amorphous Si layer to obtain an upper poly-Si layer having a random crystalline structure, as required by claim 22.

Lastly the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...depositing an amorphous intermediate layer over the lower poly-SiGe layer;

depositing an upper poly-Si layer over the amorphous intermediate layer; and

crystallizing the amorphous intermediate layer to obtain a crystallized intermediate layer having a random crystalline structure between the lower poly-SiGe layer and the upper poly-Si layer, as required by claim 30.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
August 19, 2004